Neural Network on FPGA Midterm Report

To

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# Introduction

Artificial neural networks (ANN) are a common machine learning algorithm with many real life applications. While they are often implemented in software, their parallel nature could be better implemented in hardware where parallel computations are more easily achieved. The goal of our project is to efficiently implement an ANN in a Xilinx Zynq FPGA chip by taking advantage of its concurrent functionality. We will also be investigating the tradeoffs required to implement the ANN on the FPGA. We will be comparing these results to an established, open-source ANN library implemented in C to gauge both speed and accuracy.

# Artificial Neural Networks

Artificial neural networks are loosely modeled after the structure of how neurons communicate in a brain. Neurons communicate by receiving information through the dendrite attached to its nucleus (see Figure 1). At the nucleus, if the signals trigger a reaction, it will start a chemical chain reaction which propagates down the Axon toward the dendrites of other neurons.

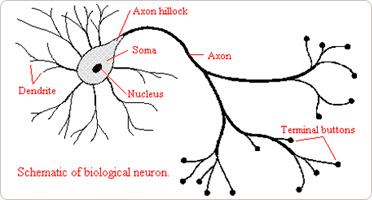


Figure 1: Example of a biological Neuron [6]

There are a number of different ways to model the neuron in an ANN. We will be using the feed-forward ANN (see Figure 2) to implement our network. In a feed-forward, the neuron is modeled as a hidden unit, which takes inputs from all of the layers before it, applies a predefined function to the inputs, and then outputs the results for the next layer to process. Our ANN will have four layers, the first layer will pass the inputs into the network to the next layer, the second and third layers will be hidden units which will process the data, and the last layer will be the output layer which will sum the results of the third layer and pass the sum out to the user.

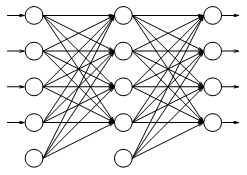


Figure 2: An example of a feed-forward ANN [5]

Artificial neural networks have been used in many applications such as stock market predictions, cancer diagnosis and many pattern recognition systems like facial recognition. The advantage of using an ANN for these types of problems is that they can be trained to predict the correct answer based on past data and results. In our implementation, we will use a method called back propagation to train our network. Back propagation relies on finding the partial derivatives of the equations that govern the network to adjust certain parameters inside the neurons to achieve a more accurate result in future iterations.

# ZYBO Zinq-7000

To implement the ANN we will be using the ZYBO Zinq-7000 development board. This board uses the Z-7010 chip which contains a 667 MHz dual-core Cortex-A9 processor as well as a programmable logic fabric equivalent to Xilinx’s Artix-7 FPGA [7]. Because the chip we are using has a processor, this will enable us to perform the complicated processes necessary to train the network in an embedded process instead of allocating additional hardware resources to training. Since our goal is to create an efficient network and not an efficient training algorithm, spending hardware resources on implementing the logic necessary to train the network will take up valuable space which could be allocated to additional units inside the network itself. This will simplify the logic design and increase the speed that the network can process data after it has been trained.

# Neural Network on an FPGA Project

## Objectives

The goal of this project was to implement an ANN on an FPGA and show that a concurrent implementation would be very efficient and could display improved performance over a serial, software neural network.

## Design Strategy

In designing an Artificial Neural Network on an FPGA, it is important to be conscientious of the algorithms that are being implemented. Relatively simple operations like multiplication or exponentials, which are common in software implementations of ANNs, are quite expensive when being implemented in hardware.

### Activation Function

Many software implementations of activation functions use Gaussian functions or exponentials in order to compute when a hidden unit has been activated or not. Both of these approaches would be prohibitively expensive on an FPGA. Our implantation will use the Elliot Activation Function, which has no exponents in it. The Elliot Activation Function is represented by the following equation: http://www4c.wolframalpha.com/Calculate/MSP/MSP1142224998e3998gh6400000h9g6b36c2e5cc85?MSPStoreType=image/gif&s=52&w=120.&h=44.

Though it doesn’t eliminate the need for multiplication and division, these operations will much less expensive that calculating exponents.

## Testing and Results

# Conclusion

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